

TECHNICAL NOTE

D-602

ADVANCED STATIC INVERTER
UTILIZING DIGITAL TECHNIQUES
AND

HARMONIC CANCELLATION

By Dorrance L. Anderson, Albert E. Willis,
and Carl E. Winkler

George C. Marshall Space Flight Center
Huntsville, Alabama

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SUMMARY

A new approach to the static inverter problem is described and analyzed. Digital techniques and unique transformer connections have been utilized to shape the output voltage wave. The three-phase output can be delta-connected and the load can be unbalanced to any extent.

The idea for the inverter described was conceived in May 1960 and a laboratory model was completed and tested successfully in February 1961. Since that time, further effort has been toward circuit simplification, refinement, and reliability.

SECTION I. INTRODUCTION

In recent years, much effort has been directed toward the development of static inverters, as power transistors and controlled rectifiers have been developed and improved. Briefly, static inverters are devices which produce alternating current from direct current without the utilization of any moving parts. They should be reliable, highly efficient, small and light, since their primary application is in missiles and satellites. The three-phase, delta-connected static inverter described in this report meets these requirements.

Investigations revealed that, presently, silicon power transistors operated as switches should be used rather than controlled rectifiers. The output waveform should be nearly sinusoidal without relying on a bulky inefficient filtering scheme as has previously been the case with static inverters.

The system of power conversion discussed here proves to have many advantages over former systems of power conversion and is far superior to rotating-type inverters. This will be more apparent as the features of this system unfold.

SECTION II. FREQUENCY STANDARD AND DIVIDER

The frequency stability required in the inverter is one part in 100,000. This is accomplished with a crystal-controlled oscillator. The oscillator is tuned to 57.6 kc and is followed by binary count-down circuits to obtain the operating frequency of 400 cycles. Eight binary stages are used. The first three stages are contained in the package with the oscillator and form a conventional counter, which divides the oscillator frequency by eight. The remaining five stages are connected in tandem and are allowed to count from 0 through 17, giving a total count of 18. During the 17 count, a reset circuit is energized and resets the counter to 0 when the 17 count disappears. This count of 18 is needed to produce the 18 steps occurring in one cycle of the 400 cycle output. This will be shown in detail later. The crystal oscillator and the first three binary stages were purchased as a package to supply 7.2 kc to the 0 to 17 counter. The departure from conventional static inverters occurs at this point. The binary stages used in the 0 to 17 counter are of the single power supply, saturating type with emitter follower outputs (Fig. 1). They are connected as a straight binary counter with the exception of a reset circuit that returns the counter to zero when the count of 17 disappears (Fig. 2). The inputs to the reset circuit are connected through resistors R_{31} and R_{32} to the \bar{A} and \bar{E} outputs of the counter. These two points are at zero potential during the time interval of count 17. During all other counts, one input or both are positive and Q_{11} is saturated. While the counter is in the 17 position, Q_{11} is cut off and C_{21} charges to the $B+$ potential through R_{33} and R_{35} (Fig. 2). At the end of the 17 count, Q_{11} is turned on and C_{21} discharges through Q_{11} and R_{35} . The negative going pulse developed across R_{35} feeds into all five binaries of the counter and sets them to the zero position. The counter continuously repeats this sequence.

SECTION III. LOGIC CIRCUITRY FOR FORMING NINE-PHASE SYSTEM

The 10 outputs of the last 5 binaries are used in proper logic circuitry to form 9 functions as shown by the truth table in Figure 3. The truth table shows the binary numbers 0 to 17 in sequence, reading from top to bottom. The next count after 17 is zero again, as previously explained. Figure 1 shows the five flip-flops being considered. Their condition at any time can be determined from the truth table under A, B, C, D, or E, where A is the most significant and E the least. Column m denotes the particular minterm and this number agrees with the binary number in each case. The desired functions were next written into the truth table in such a manner as to produce nine square waves of voltage at intervals of $\frac{2\pi}{9}$ radians. This can effectively be accomplished by producing nine square waves of voltage at intervals of $\frac{\pi}{9}$ radians during one half cycle of the 0-17 counter. It must be kept in mind that the primed functions f_6 , f_7 , f_8 , and f_9 must be inverted if an interval of $\frac{2\pi}{9}$ radians is to exist between successively numbered phases and they must be treated accordingly.

The Boolean equation of each function can now be written from the information contained in the truth table and the simplest expression can be determined through the use of the Veitch diagram. For example, function

$$f_1 = \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}\bar{B}\bar{C}D\bar{E} + \bar{A}\bar{B}\bar{C}DE + \bar{A}\bar{B}C\bar{D}\bar{E} + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CD\bar{E} + \bar{A}\bar{B}CDE \\ + \bar{A}B\bar{C}\bar{D}\bar{E} \quad (1)$$

This can also be written

$$f_1 = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 \quad (2)$$

That is, wherever a "1" appears under f_1 in the truth table, the proper AND and OR circuitry should be set up to fulfill the Boolean expression. If diode logic is used, this would require 54 diodes for f_1 . If AND circuits were set up for minterms 0 through 16, 85 diodes would be necessary. The 9 OR circuits would each require 9 diodes or 81 for all 9. The total number of diodes in this kind of arrangement would be 166. Fortunately, a valuable and powerful device known as a Veitch diagram greatly simplifies the Boolean expressions of the nine functions; therefore, the number of diodes required are reduced to a fraction of the 166 previously mentioned. Figure 4 shows a Veitch diagram for 5 variables A, B, C, D, and E with the minterms properly

located. For our particular counter, minterms 18 through 31 are redundant; therefore, an "x" can be placed on the Veitch diagram wherever these terms occur and these can be used in simplification. For function f_1 , for example, minterms 0 through 8 are placed on the diagram by inserting "1's" in the proper squares. Now by making valid minterm combinations wherever the "1's" and "x's" occur on the diagram, the Boolean expression of equation (1) is reduced to

$$f_1 = \bar{A}\bar{B} + \bar{A}\bar{C}\bar{D}\bar{E} \quad (3)$$

This requires 8 diodes instead of 54 as was the case prior to simplification. Looking at the diagram, minterms 0 through 7 combine to form $\bar{A}\bar{B}$ and minterms 0 and 8 combine to form $\bar{A}\bar{C}\bar{D}\bar{E}$. In a similar manner, each of the other eight functions is simplified. The Veitch diagrams of these functions are shown in Figure 5. Figure 6 shows a block diagram of the logic that has been discussed and Figure 7 shows a diode logic circuit to produce these functions.

Resistor-transistor logic (RTL) is used in place of the diode logic already discussed since this has the added advantage of providing additional gain, thereby minimizing the gain requirements of the nine power amplifiers. Worst-case design techniques were used in designing all logic circuitry. Figure 8 shows the RTL arrangement.

SECTION IV. PHASE INVERTER AND POWER AMPLIFIERS

The output signals from the second level logic transistors are single-ended. Therefore, a phase inverter must be used to produce push-pull signals for driving the power amplifiers. This is achieved as shown in Figure 8. The base of Q_1 is connected to the collector of Q_2 through R_1 . When Q_2 is driven to saturation, its collector drops to a very low potential and Q_1 is cut off. If Q_2 is off, its collector becomes positive and drives Q_1 to saturation. Q_1 and Q_2 are operated at sufficient power levels to drive the power amplifiers to the required output. The power amplifiers are conventional switching amplifiers operating square wave. For efficiency and reliability, this is an ideal mode of operation. The power amplifiers differ only in the design of output transformers. Since the output transformers are quite unique, their design will be covered in some detail.

SECTION V. OUTPUT TRANSFORMER DESIGN, CONNECTIONS, AND WAVESHAPING

A stepped wave that closely approximates a sine wave can be formed by dividing a sine wave into a number of equal intervals along the x-axis, integrating the sine wave over these intervals, and dividing the resultant by the x interval. This gives the amplitude of the various steps of the stepped wave. If the equation of the sine wave is

$$y = Y \sin x$$

then the general expression for the amplitudes of the various steps of the stepped wave would be

$$y_k = \frac{NY}{2\pi} \int_{(k-1) \frac{2\pi}{N}}^{k \frac{2\pi}{N}} \sin x \, dx \quad (5)$$

where $N = 3n$ and n goes from 1 to ∞ . The value of k goes from 1 to N . Figure 10 shows the stepped wave for $N = 18$.

Inspection of equation (5) for y_k reveals that the stepped wave, $f(x)$, is ODD since

$$f(-x) = -f(x). \quad (6)$$

Therefore, it can be said that only sine terms appear in a Fourier expansion of $f(x)$.

$$f(x) = \sum_{m=1}^{\infty} b_m \sin mx. \quad (7)$$

The coefficients of the sine terms (b_m) can be found from

$$b_m = \frac{1}{\pi} \int_0^{2\pi} f(x) \sin mx \, dx \quad (8)$$

and since $f(x) = y_k$ between the limits outlined the following expression for b_m is valid.

$$b_m = \frac{NY}{2\pi^2} \cdot \sum_{k=1}^N \int_{(k-1)\frac{2\pi}{N}}^{k\frac{2\pi}{N}} \sin x \, dx \cdot \int_{(k-1)\frac{2\pi}{N}}^{k\frac{2\pi}{N}} \sin mx \, dx \quad (9)$$

$$= \frac{NY}{2\pi^2} \cdot \sum_{k=1}^N \left[\cos (k-1) \frac{2\pi}{N} - \cos k \frac{2\pi}{N} \right] \cdot \left[\cos (k-1) \frac{2\pi m}{N} - \cos \frac{2\pi m}{N} \right] \quad (10)$$

$$= \frac{4NY}{2\pi^2} \cdot \sum_{k=1}^N \sin \frac{\pi}{N} \cdot \sin \frac{\pi m}{N} \cdot \sin (2k-1) \frac{\pi}{N} \cdot \sin (2k-1) \frac{\pi m}{N} \quad (11)$$

$$= \frac{NY}{2\pi^2} \cdot \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right] \cdot \sum_{k=1}^N \left[\cos (2k-1) \frac{m-1}{N} \pi - \cos (2k-1) \frac{m+1}{N} \pi \right] \quad (12)$$

Now, since $\cos \alpha$ is the real part of $e^{i\alpha}$, we can write the following:

$$b_m = \frac{NY}{2\pi^2 m} \cdot \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right] \\ \cdot \sum_{k=1}^N \operatorname{Re} \left[e^{(2k-1) \frac{m-1}{N} \pi i} - e^{(2k-1) \frac{m+1}{N} \pi i} \right] \quad (13)$$

$$= \frac{NY}{2\pi^2 m} \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right] \\ \cdot \operatorname{Re} \left[e^{-\frac{(m-1)}{N} \pi i} \cdot \sum_{k=0}^{N-1} e^{\frac{(m-1)}{N} 2\pi i k} - e^{-\frac{(m+1)}{N} \pi i} \cdot \sum_{k=0}^{N-1} e^{\frac{(m+1)}{N} 2\pi i k} \right] \quad (14)$$

The summation for $k = 0$ to $k = N-1$ is the same as for $k = 1$ to $k = N$.

Now the following is true:

$$\sum_{k=0}^{N-1} e^{\frac{m-1}{N} 2\pi i k} = \begin{cases} N, & \text{if } \frac{m-1}{N} \text{ is an integer} \\ 0, & \text{if } \frac{m-1}{N} \text{ is not an integer} \end{cases} \quad (15)$$

and

$$\sum_{k=0}^{N-1} e^{\frac{m+1}{N} 2\pi i k} = \begin{cases} N, & \text{if } \frac{m+1}{N} \text{ is an integer} \\ 0, & \text{if } \frac{m+1}{N} \text{ is not an integer} \end{cases} \quad (16)$$

A consideration of the following will make this clearer.

$$\sum_{k=0}^{N-1} e^{\frac{a}{N} 2\pi i k} = \frac{1 - e^{2\pi i a}}{1 - e^{2\pi i \frac{a}{N}}} \quad (17)$$

If $\frac{a}{N}$ is an integer, $e^{\frac{a}{N} 2\pi i k} = 1$, therefore $\sum_{k=0}^{N-1} e^{\frac{a}{N} 2\pi i k} = N$

is an integer. (18)

When $\frac{a}{N}$ is not an integer the denominator of equation (17) is some value other than zero, but the numerator is zero, therefore,

$$\sum_{k=0}^{N-1} e^{\frac{a}{N} 2\pi i k} = 0 \quad \text{when } \frac{a}{N} \text{ is not an integer.} \quad (19)$$

In the above discussion an integer can be 0 or any positive whole number.

Since $N = 3n$ and the smallest value for n is one, it can be said that $N \geq 3$. This means that $\frac{m-1}{N}$ and $\frac{m+1}{N}$ cannot be integers simultaneously. They can, obviously, both be non-integers at the same time.

Thus,

$$b_m = \frac{N^2 Y}{2\pi^2 m} \cdot \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right]$$

$$\begin{cases} \cos \frac{m-1}{N} \pi, & \text{if } \frac{m-1}{N} \text{ is an integer} \\ -\cos \frac{m+1}{N} \pi, & \text{if } \frac{m+1}{N} \text{ is an integer} \\ 0, & \text{if both are non-integers} \end{cases} \quad (20)$$

Let $\frac{m-1}{N}$ be an integer ℓ

$$\frac{m-1}{N} = \ell, \text{ then } \frac{m+1}{N} = \ell + \frac{2}{N} \quad (21)$$

$$\begin{aligned} \cos \frac{m+1}{N} \pi &= \cos \left(\ell + \frac{2}{N} \right) \pi = \cos \ell \pi \cdot \cos \frac{2\pi}{N} \\ &= (-1)^\ell \cos \frac{2\pi}{N}. \end{aligned} \quad (22)$$

Therefore,

$$\begin{aligned} \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right] \cdot \cos \frac{m-1}{N} \pi &= \left[(-1)^\ell - (-1)^\ell \cos \frac{2\pi}{N} \right] \cdot \\ &(-1)^\ell = 1 - \cos \frac{2\pi}{N}. \end{aligned} \quad (23)$$

Let $\frac{m+1}{N}$ be an integer ℓ

$$\frac{m+1}{N} = \ell, \text{ then } \frac{m-1}{N} = \ell - \frac{2}{N} \quad (24)$$

$$\cos \frac{m-1}{N} \pi = \cos \left(\ell - \frac{2}{N} \right) \pi = \cos \ell \pi \cdot \cos \frac{2\pi}{N} = (-1)^\ell \cos \frac{2\pi}{N}. \quad (25)$$

Therefore,

$$\begin{aligned} \left[\cos \frac{m-1}{N} \pi - \cos \frac{m+1}{N} \pi \right] \cdot \left(-\cos \frac{m+1}{N} \pi \right) &= \left[(-1)^\ell \cos \frac{2\pi}{N} - (-1)^\ell \right] \cdot \\ &\left[-(-1)^\ell \right] = 1 - \cos \frac{2\pi}{N}. \end{aligned} \quad (26)$$

Hence,

$$b_m = \frac{N^2 Y}{2\pi^2 m} \left(1 - \cos \frac{2\pi}{N}\right) = \frac{Y}{m} \left(\frac{N}{\pi} \sin \frac{\pi}{N}\right)^2 \quad \text{if } m \equiv \pm 1 \pmod{N} \quad (27)$$

$$b_m = 0 \quad \text{otherwise} \quad (28)$$

$$b_1 = Y \left(\frac{N}{\pi} \sin \frac{\pi}{N}\right)^2 \quad (29)$$

$$b_m = \frac{b_1}{m} \quad (30)$$

The stepped wave is described by the Fourier series

$$f(x) = b_1 \left\{ \sin x + \sum_{p=1}^{\infty} \left[\frac{1}{pN-1} \sin(pN-1)x + \frac{1}{pN+1} \sin(pN+1)x \right] \right\} \quad (31)$$

This wave is now shifted forward by $\frac{2\pi}{3}$ radians and backward the same amount; the two equations are

$$f\left(x + \frac{2\pi}{3}\right) = b_1 \left\{ \sin\left(x + \frac{2\pi}{3}\right) + \sum_{p=1}^{\infty} \left[\frac{1}{pN-1} \sin(pN-1)\left(x + \frac{2\pi}{3}\right) + \frac{1}{pN+1} \sin(pN+1)\left(x + \frac{2\pi}{3}\right) \right] \right\} \quad (32)$$

$$f\left(x - \frac{2\pi}{3}\right) = b_1 \left\{ \sin\left(x - \frac{2\pi}{3}\right) + \sum_{p=1}^{\infty} \left[\frac{1}{pN-1} \cdot \sin(pN-1)\left(x - \frac{2\pi}{3}\right) + \frac{1}{pN+1} \cdot \sin(pN+1)\left(x - \frac{2\pi}{3}\right) \right] \right\} \quad (33)$$

$$\sin\left(x + \frac{2\pi}{3}\right) = -\frac{1}{2} \sin x + \frac{\sqrt{3}}{2} \cos x \quad (34)$$

$$\sin\left(x - \frac{2\pi}{3}\right) = -\frac{1}{2} \sin x - \frac{\sqrt{3}}{2} \cos x \quad (35)$$

$$\sin x + \sin\left(x + \frac{2\pi}{3}\right) + \sin\left(x - \frac{2\pi}{3}\right) = 0 \quad (36)$$

$$\sum_{p=1}^{\infty} \sin(pN-1)x = \sum_{p=1}^{\infty} [\sin pNx \cdot \cos x - \cos pNx \cdot \sin x] \quad (37)$$

$$\sum_{p=1}^{\infty} \sin(pN-1)\left(x - \frac{2\pi}{3}\right) = \sum_{p=1}^{\infty} \left[-\frac{1}{2} \cos x \cdot \sin pNx + \frac{\sqrt{3}}{2} \sin x \cdot \sin pNx + \frac{1}{2} \sin x \cdot \cos pNx + \frac{\sqrt{3}}{2} \cos x \cdot \cos pNx \right] \quad (38)$$

$$\sum_{p=1}^{\infty} \sin(pN-1)\left(x + \frac{2\pi}{3}\right) =$$

$$\sum_{p=1}^{\infty} \left[-\frac{1}{2} \cos x \cdot \sin pNx - \frac{\sqrt{3}}{2} \sin x \cdot \sin pNx + \frac{1}{2} \sin x \cdot \cos pNx - \frac{\sqrt{3}}{2} \cos x \cdot \cos pNx \right] \quad (39)$$

$$\sum_{p=1}^{\infty} \left[\sin(pN-1)x + \sin(pN-1)\left(x - \frac{2\pi}{3}\right) + \sin(pN-1)\left(x + \frac{2\pi}{3}\right) \right] = 0 \quad (40)$$

Similarly

$$\sum_{p=1}^{\infty} \left[\sin(pN+1)x + \sin(pN+1)\left(x - \frac{2\pi}{3}\right) + \sin(pN+1)\left(x + \frac{2\pi}{3}\right) \right] = 0 \quad (41)$$

Therefore,

$$f(x) + f\left(x + \frac{2\pi}{3}\right) + f\left(x - \frac{2\pi}{3}\right) = 0. \quad (42)$$

The significance of this fact is that when these three stepped waves are actual voltages, they can be connected in delta with theoretically zero resultant voltage.

Next, the total harmonic content of the stepped wave will be determined. The effective value of the stepped wave is given by

$$\text{EFFECTIVE VALUE OF STEPPED WAVE} = \sqrt{\frac{\frac{2\pi}{N} \cdot \sum_{k=1}^N (y_k)^2}{2\pi}} \quad (43)$$

where

$$y_k = \frac{NY}{2\pi} \left[\cos(k-1) \frac{2\pi}{N} - \cos k \frac{2\pi}{N} \right] \quad (44)$$

$$= \frac{NY}{\pi} \sin(2k-1) \frac{\pi}{N} \cdot \sin \frac{\pi}{N} \quad (45)$$

$$\text{EFFECTIVE VALUE OF STEPPED WAVE} = \sqrt{\frac{NY^2}{\pi^2} \cdot \sin^2 \frac{\pi}{N} \cdot \sum_{k=0}^{N-1} \sin^2 (2k-1) \frac{\pi}{N}} \quad (46)$$

$$\begin{aligned} \sum_{k=0}^{N-1} \sin^2 (2k-1) \frac{\pi}{N} &= \sum_{k=0}^{N-1} \left[\frac{1 - \cos (2k-1) \frac{2\pi}{N}}{2} \right] \\ &= \frac{N}{2} - \frac{1}{2} \sum_{k=0}^{N-1} \operatorname{Re} \left[e^{(2k-1) \frac{2\pi}{N} i} \right] \end{aligned} \quad (47)$$

$$= \frac{N}{2} - \frac{1}{2} \cdot e^{-\frac{2\pi i}{N}} \cdot \operatorname{Re} \sum_{k=0}^{N-1} e^{\frac{4k\pi i}{N}} \quad (48)$$

$$\sum_{k=0}^{N-1} e^{\frac{4k\pi i}{N}} = \frac{1 - e^{\frac{4\pi i}{N}}}{1 - e^{\frac{4\pi i}{N}}} = 0 \quad \begin{array}{l} \text{since } N \text{ is a multiple of } 3 \\ \text{and } \frac{4}{N} \text{ cannot be an integer} \end{array} \quad (49)$$

Therefore

$$\sum_{k=0}^{N-1} \sin^2 (2k-1) \frac{\pi}{N} = \frac{N}{2} \quad (50)$$

and

$$\text{EFFECTIVE VALUE OF STEPPED WAVE} = \sqrt{\frac{NY^2}{2\pi^2} \cdot \sin^2 \frac{\pi}{N}} = \sqrt{\frac{b_1 Y}{2}} \quad (51)$$

$$\begin{array}{l} \text{EFFECTIVE VALUE OF} \\ \text{FUNDAMENTAL} \end{array} = \frac{b_1}{\sqrt{2}} \quad (52)$$

The effective value of the stepped wave can also be determined by considering the harmonic amplitudes given in the Fourier series.

$$\sqrt{\frac{b_1 Y}{2}} = \sqrt{\frac{b_1^2}{2} + \frac{\left[\sum_{p=1}^{\infty} \frac{b_1}{pN-1} \right]^2}{2} + \frac{\left[\sum_{p=1}^{\infty} \frac{b_1}{pN+1} \right]^2}{2}} \quad (53)$$

Therefore

$$\sqrt{\frac{b_1 Y}{2} - \frac{b_1^2}{2}} = \sqrt{\frac{\left[\sum_{p=1}^{\infty} \frac{b_1}{pN-1} \right]^2}{2} + \frac{\left[\sum_{p=1}^{\infty} \frac{b_1}{pN+1} \right]^2}{2}} \quad (54)$$

The right-hand side of this equation is precisely the effective value of the resultant wave when the fundamental or first harmonic is eliminated from the stepped wave. In other words, the right-hand side of this equation is an effective value for all harmonics higher than the first. The total harmonic content of the stepped wave can now be expressed as a percentage.

$$\% \text{ TOTAL HARMONIC CONTENT} = \frac{\text{EFFECTIVE VALUE OF HIGHER HARMONICS}}{\text{EFFECTIVE VALUE OF FUNDAMENTAL}} \times 100 \quad (55)$$

$$= \frac{\sqrt{\frac{b_1 Y}{2} - \frac{b_1^2}{2}}}{\frac{b_1}{\sqrt{2}}} \times 100 = \sqrt{\frac{Y}{b_1} - 1} \times 100 = \sqrt{\frac{1}{\left(\frac{N}{\pi} \sin \frac{\pi}{N}\right)^2} - 1} \times 100 \quad (56)$$

Since the static inverter that has been developed has 18 steps in its output voltage wave, the case where $N = 18$ will be discussed in detail.

The original sine wave of Figure 10 can be written as a voltage

$$v = V \sin \omega t. \quad (57)$$

The equation of the stepped wave voltage then becomes

$$v' = V_1 \left\{ \sin \omega t + \sum_{p=1}^{\infty} \left[\frac{1}{18p-1} \cdot \sin (18p-1) \omega t + \frac{1}{18p+1} \cdot \sin (18p+1) \omega t \right] \right\} \quad (58)$$

where, V_1 , the amplitude of the fundamental voltage is

$$V_1 = V \left(\frac{18}{\pi} \sin \frac{\pi}{18} \right)^2 \quad (59)$$

The effective value of the fundamental voltage is

$$\left(V_1 \right)_{\text{EFF}} = \frac{V_1}{\sqrt{2}} = \frac{V}{\sqrt{2}} \cdot \left(\frac{18}{\pi} \sin \frac{\pi}{18} \right)^2. \quad (60)$$

Equation (5) can be used to find the amplitudes of the various steps of the stepped wave and these amplitudes can be expressed as voltages.

$$v_1 = v_9 = -v_{10} = -v_{18} = \frac{\pi}{18} \cdot V_1 \cdot \frac{\sin \frac{\pi}{18}}{\sin \frac{\pi}{18}} = \frac{\pi}{18} \cdot V_1 \quad (61)$$

$$v_2 = v_8 = -v_{11} = -v_{17} = \frac{\pi}{18} \cdot V_1 \cdot \frac{\sin \frac{3\pi}{18}}{\sin \frac{\pi}{18}} = \frac{\pi}{18} \cdot \frac{1}{2} \cdot V_1 \quad (62)$$

$$v_3 = v_7 = -v_{12} = -v_{16} = \frac{\pi}{18} \cdot V_1 \cdot \frac{\sin \frac{5\pi}{18}}{\sin \frac{\pi}{18}} = \frac{\pi}{18} \cdot \frac{\sin \frac{5\pi}{18}}{\sin \frac{\pi}{18}} \cdot V_1 \quad (63)$$

$$v_4 = v_6 = -v_{13} = -v_{15} = \frac{\pi}{18} \cdot V_1 \cdot \frac{\sin \frac{7\pi}{18}}{\sin \frac{\pi}{18}} = \frac{\pi}{18} \cdot \frac{\sin \frac{7\pi}{18}}{\sin \frac{\pi}{18}} \cdot V_1 \quad (64)$$

$$v_5 = -v_{14} = \frac{\pi}{18} \cdot V_1 \cdot \frac{\sin \frac{9\pi}{18}}{\sin \frac{\pi}{18}} = \frac{\pi}{18} \cdot \frac{1}{\sin \frac{\pi}{18}} \cdot V_1 \quad (65)$$

y_k of equation (5) is replaced by v_k since actual voltages are now being considered.

The desired step wave for the output voltage with the proper amplitude for the steps can be formed by combining the square-wave voltages of the required amplitude as furnished by the nine phases. This is shown in Figure 11. The amplitudes of these voltages can now be shown.

$$V_a = v_1 = \frac{\pi}{18} \cdot V_1 = \frac{\pi\sqrt{2}}{18} \cdot (V_1)_{\text{EFF}} \quad (66)$$

$$V_b = \frac{v_2 - v_1}{2} = \frac{\pi}{18} \cdot V_1 \cdot \cos \frac{\pi}{9} = \frac{\pi\sqrt{2}}{18} \cdot \cos \frac{\pi}{9} \cdot (V_1)_{\text{EFF}} \quad (67)$$

$$V_c = \frac{v_3 - v_2}{2} = \frac{\pi}{18} \cdot V_1 \cdot \cos \frac{2\pi}{9} = \frac{\pi\sqrt{2}}{18} \cdot \cos \frac{2\pi}{9} \cdot (V_1)_{\text{EFF}} \quad (68)$$

$$V_d = \frac{v_4 - v_3}{2} = \frac{\pi}{18} \cdot V_1 \cdot \frac{1}{2} = \frac{\pi \sqrt{2}}{36} \cdot (V_1)_{\text{EFF}} \quad (69)$$

$$V_e = \frac{v_5 - v_4}{2} = \frac{\pi}{18} \cdot V_1 \cdot \cos \frac{4\pi}{9} = \frac{\pi \sqrt{2}}{18} \cdot \cos \frac{4\pi}{9} \cdot (V_1)_{\text{EFF}} \quad (70)$$

If the transformers are considered ideal, that is, if losses are neglected, expressions can be shown to determine the primary and secondary numbers of turns.

$$N_p = \frac{V_{\text{DC}} \times 10^8}{4 \cdot B \cdot A \cdot f} \quad (71)$$

where:

N_p = one-half of the primary turns

V_{DC} = the d.c. voltage applied to the center-tapped primary

B = the flux density of the core material in gauss

A = the effective cross-sectional area of the core in cm^2

f = the frequency in cycles per second

$$N_a = N_p \cdot \frac{V_a}{V_{\text{DC}}} = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{\text{EFF}}}{18 \cdot V_{\text{DC}}} \quad (72)$$

$$N_b = N_p \cdot \frac{V_b}{V_{\text{DC}}} = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{\text{EFF}}}{18 \cdot V_{\text{DC}}} \cdot \cos \frac{\pi}{9} = N_a \cdot \cos \frac{\pi}{9} \quad (73)$$

$$N_c = N_p \cdot \frac{V_c}{V_{\text{DC}}} = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{\text{EFF}}}{18 \cdot V_{\text{DC}}} \cdot \cos \frac{2\pi}{9} = N_a \cdot \cos \frac{2\pi}{9} \quad (74)$$

$$N_d = N_p \cdot \frac{V_d}{V_{DC}} = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{EFF}}{18 \cdot V_{DC}} \cdot \frac{1}{2} = N_a \cdot \frac{1}{2} \quad (75)$$

$$N_e = N_p \cdot \frac{V_e}{V_{DC}} = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{EFF}}{18 \cdot V_{DC}} \cdot \cos \frac{4\pi}{9} = N_a \cdot \cos \frac{4\pi}{9} \quad (76)$$

The primaries of all nine output transformers are identical having $2N_p$ turns with a center tap. Preferably, the primaries are bifilar wound. The Type I transformer has one secondary winding of N_a turns and two secondary windings of N_d turns. The Type II transformer has one secondary winding of N_b turns, one of N_c turns, and one of N_e turns.

In practice, some allowance should be made for transformer core and copper losses. When the effective phase voltage $(V_1)_{EFF}$ is specified and the d.c. voltage V_{DC} is set, all that is necessary is to choose a transformer core that will handle the required power at the specified frequency.

As shown in Figure 9, there are three transformers of Type I and six of Type II. If the inverter is properly designed, the three-phase output can be delta-connected as shown and the resultant voltage is theoretically zero as previously proved. Since fractions of turns are not possible, however, there is a likelihood that a resultant voltage will be present. Ingenuity on the part of the designer can minimize this voltage to a point where it can be neglected.

The number of steps of the output wave must be a multiple of three if the three phases of a three-phase system are to be connected in delta. This was the reason for setting $N = 3n$ where n went from 1 to ∞ in equation (5).

The interconnection of three secondaries on each of the nine output transformers must next be considered. Since the steps occur at intervals of $\frac{\pi}{9}$ radians or every 20 degrees, phase A voltage, V_A , can be built up thusly.

$$V_A = (V_a)_1 + (V_b)_8 + (V_c)_2 + (V_d)_7 + (V_e)_3 - (V_e)_8 - (V_d)_4 - (V_c)_9 - (V_b)_5 \quad (77)$$

$$\begin{aligned}
&= (v_a)_1 - (v_b)_6 + (v_c)_2 - (v_d)_7 + (v_e)_3 + (v_e)_8 - (v_d)_4 + (v_c)_9 \\
&- (v_b)_5
\end{aligned} \tag{78}$$

The first expression for V_A can be followed directly on the connection diagram, Figure 9. As previously explained when discussing the formation of the nine functions, those voltages with the primed subscripts must be inverted to form a balanced nine-phase system of square-wave voltages. When these voltages are inverted, the primes are removed and there are $\frac{2\pi}{9}$ radians between voltages with consecutive subscripts. Thus, we have the second equation for V_A which says that when we have nine phases of square waves with 40 degrees between adjacently numbered phases, V_A is formed by subtracting V_d of phase 4, V_b of phase 5, V_b of phase 6, and V_d of phase 7 from the sum of V_a of phase 1, V_c of phase 2, V_e of phase 3, V_e of phase 8, and V_c of phase 9.

Similarly:

$$\begin{aligned}
v_B &= (v_a)_4 + (v_b)_{9'} + (v_c)_5 + (v_d)_{1'} + (v_e)_6 - (v_e)_{2'} - (v_d)_7 - (v_c)_{3'} \\
&- (v_b)_8
\end{aligned} \tag{79}$$

$$\begin{aligned}
&= (v_a)_4 - (v_b)_9 + (v_c)_5 - (v_d)_1 + (v_e)_6 + (v_e)_2 - (v_d)_7 + (v_c)_3 \\
&- (v_b)_8
\end{aligned} \tag{80}$$

$$\begin{aligned}
v_C &= (v_a)_7 + (v_b)_{3'} + (v_c)_8 + (v_d)_{4'} + (v_e)_9 - (v_e)_{5'} - (v_d)_1 - (v_c)_{6'} \\
&- (v_b)_2
\end{aligned} \tag{81}$$

$$= \left(V_a \right)_7 - \left(V_b \right)_3 + \left(V_c \right)_8 - \left(V_d \right)_4 + \left(V_e \right)_9 + \left(V_e \right)_5 - \left(V_d \right)_1 + \left(V_c \right)_6 - \left(V_b \right)_2 \quad (82)$$

Figures 12, 13, 14, and 15 are included for the case where $N = 30$

The number of turns for the transformer primaries can be found from equation (71). In this case, there are three types of transformers R, S, and T. As before, the primaries of all 15 transformers are identical. There are three transformers of Type R, having secondary windings N_a , N_f , and N_i . There are six transformers of Type S, having secondary windings N_b , N_e , and N_g . There are six transformers of Type T, having secondary windings N_c , N_d , and N_h .

These secondary numbers of turns are given by

$$N_a = \frac{\pi \sqrt{2} \cdot N_p \cdot (V_1)_{EFF}}{30 V_{DC}} \quad (83)$$

$$N_b = N_a \cdot \cos \frac{\pi}{15} \quad (84)$$

$$N_c = N_a \cdot \cos \frac{2\pi}{15} \quad (85)$$

$$N_d = N_a \cdot \cos \frac{3\pi}{15} \quad (86)$$

$$N_e = N_a \cdot \cos \frac{4\pi}{15} \quad (87)$$

$$N_f = N_a \cdot \frac{1}{2} \quad (88)$$

$$N_g = N_a \cdot \cos \frac{6\pi}{15} \quad (89)$$

$$N_h = N_a \cdot \cos \frac{7\pi}{15} \quad (90)$$

The 15 transformers are shown properly interconnected to produce a three-phase system of stepped waves connected in delta.

Equation (56) was calculated for several values of N and the results are tabulated.

N	% TOTAL HARMONIC CONTENT
3	67.98
6	31.08
9	20.40
12	15.22
15	12.15
18	10.11
21	8.66
24	7.57
27	6.73
30	6.05
33	5.50
36	5.04
39	4.65
42	4.32
45	4.03

This data is plotted in Figure 17.

SECTION VI: VOLTAGE REGULATION

The dc voltage regulating scheme is shown in Figure 16. The dc to the power output amplifiers is controlled by adding a small dc voltage to the existing dc supply. The small dc voltage supplies approximately one-quarter of the input power under extreme conditions; that is, when the existing dc supply is low in voltage for any reason and also when the inverter is being required to handle a full load.

The three-phase output voltage is full-wave rectified and fed to a zener diode bridge circuit. The variable resistor in the bridge circuit is used to set the control current in a conventional two-core dc magnetic amplifier of the self-saturating type. Two stages of transistor amplification follow the magnetic amplifier. The output of this last stage is full-wave rectified, filtered, and added to the existing dc supply. The combination of the existing dc supply voltage and the additional voltage provides the dc for the nine power amplifiers of the inverter.

It can be seen from the truth table of Figure 3 that the output of flip-flop E in the binary countdown circuit is a symmetrical square wave. The frequency of the output of flip-flop E would be 3.6 kc for a 400 cps inverter. If this 3.6 kc is divided down twice through binary circuitry, a 900-cps square wave results. It can be seen in Figure 16 that this voltage is amplified to be used for ac excitation of the magnetic amplifier.

The power transistors of the output stage of the dc regulatory circuit are pulse-width modulated since they are driven from the magnetic amplifier. A more desirable mode of operation would be full square-wave switching; in fact, a dc regulator incorporating this has been developed with a resultant increase in efficiency. This system contains two power amplifiers, one of which is shifted in phase with respect to the other to obtain control. Normally, it can be figured that about one-fourth of the input power is furnished by the dc regulator. In this case, each of the two power amplifiers needs to furnish only one-eighth of the power. With presently available power transistors and using a dc regulator of this type in an inverter circuit where the output wave has steps at 12-degree intervals, a unit having a rating of 7500 va is entirely feasible and paralleling of power transistors is unnecessary.

An improved voltage control system now under development will no doubt be used on static inverters of the future. Briefly, two three-phase static inverters are built up and their transformer secondaries are interconnected in such a way as to produce a three-phase system whose voltage can be varied by shifting one inverter in phase with respect to the other. This system should be more efficient than any other system used so far. It has the additional important feature that if the inverter output is shorted, one inverter will shift 180 degrees with respect to the other, producing a zero-output voltage across the short circuit. When the short is removed, normal operation proceeds.

SECTION VII. DISCUSSION OF A 1000 VA STATIC INVERTER

A three-phase, 115-volt, 400-cps, 1,000-va static inverter was designed and built up. The output voltage wave contained 18 steps and the inverter was delta-connected. Figure 18 shows a picture of the output wave. Conservative, worst-case design techniques were used throughout to insure maximum reliability. The normal battery voltage was 56 volts, but for changes in battery voltage from 50 volts to 60 volts, the average of the three output voltages was held to within 0.5 volts of the rated 115 volts from no-load to nearly 100-percent overload. The unit was run continuously at 50-percent overload without excessive heating. The frequency was crystal-controlled and accurate to 0.0015 percent over the temperature range of the tests which was 0 degrees centigrade to 60 degrees centigrade.

Figure 19 shows a plot of the over-all efficiency of this static inverter as a function of load. The battery voltage was held constant at 56 volts. A slight increase in efficiency is experienced for higher battery voltages and a slight decrease in efficiency results from lower battery voltages, since the amount of input power furnished by the voltage regulator is inversely proportional to the battery voltage.

The inverter output voltage was measured as a full 1,000-va load was switched on and off. When the inverter was required to suddenly go from no-load condition to full-load, the output voltage dropped from the normal 115 volts to 100 volts and recovered to 115 volts again in 3 cycles or 7.5 milliseconds. When this 1,000-va load was suddenly removed the output voltage rose to 128 volts and recovered to 115 volts in 10 cycles or 25 milliseconds.

SECTION VIII. CONCLUSIONS

The unique features and advantages of this approach to static power supplies can be stated, but not necessarily in their order of importance.

1. When the stepped wave is properly formed, the first harmonic present is determined by the number of steps and is one less than the number of steps per cycle. That is, with an 18-step, 400-cps inverter the first harmonic is the 17th, or 6.8 kc.

2. The method of forming the stepped wave keeps the total harmonic content to a minimum.

3. The three-phase output can be delta-connected if desired, since the sum of the three output voltages is zero at any instant, as is the case with pure sine waves.

4. The power transistors are fully switched throughout. This, of course, is the most efficient mode of operation.

5. A bulky waveshaping filter is not required in the output because of the low harmonic content. This saves on over-all weight.

6. The dc regulating scheme is quite efficient since the full battery voltage can be utilized directly, and only a small voltage that is added to the battery needs to be controlled.

7. The frequency is crystal controlled.

8. The circuit contains no moving parts; therefore, no maintenance is required.

9. The device is highly reliable since worst-case design techniques were employed in the design of all of the logic circuitry and extensive tests have been made from -40 degrees centigrade to + 70 degrees centigrade without any failure.

10. Unbalanced loads are easily handled since the power amplifiers inherently share the load.

11. The device is small and light, making it ideal for missiles and satellites.

12. All previous conclusions are valid for the case where the limits of equation (5) are changed to include the x-interval $(2K - 1) \frac{\pi}{N}$ to $(2K + 1) \frac{\pi}{N}$. The value of K goes from $K = 0$ to $K = N - 1$. This would alter the output stepped wave slightly, producing steps of zero amplitude along the x-axis between $-\frac{\pi}{N}$ and $+\frac{\pi}{N}$. The consequence of this would be to change the output transformer design slightly with a resultant simplification of transformer manufacturing in certain cases.

The authors would like to express their thanks to Dr. R. F. Schulz-Arenstorff of the Computation Division for his assistance in the development of equations (13) through (27). It is felt that his efforts greatly enhance the value of this paper.

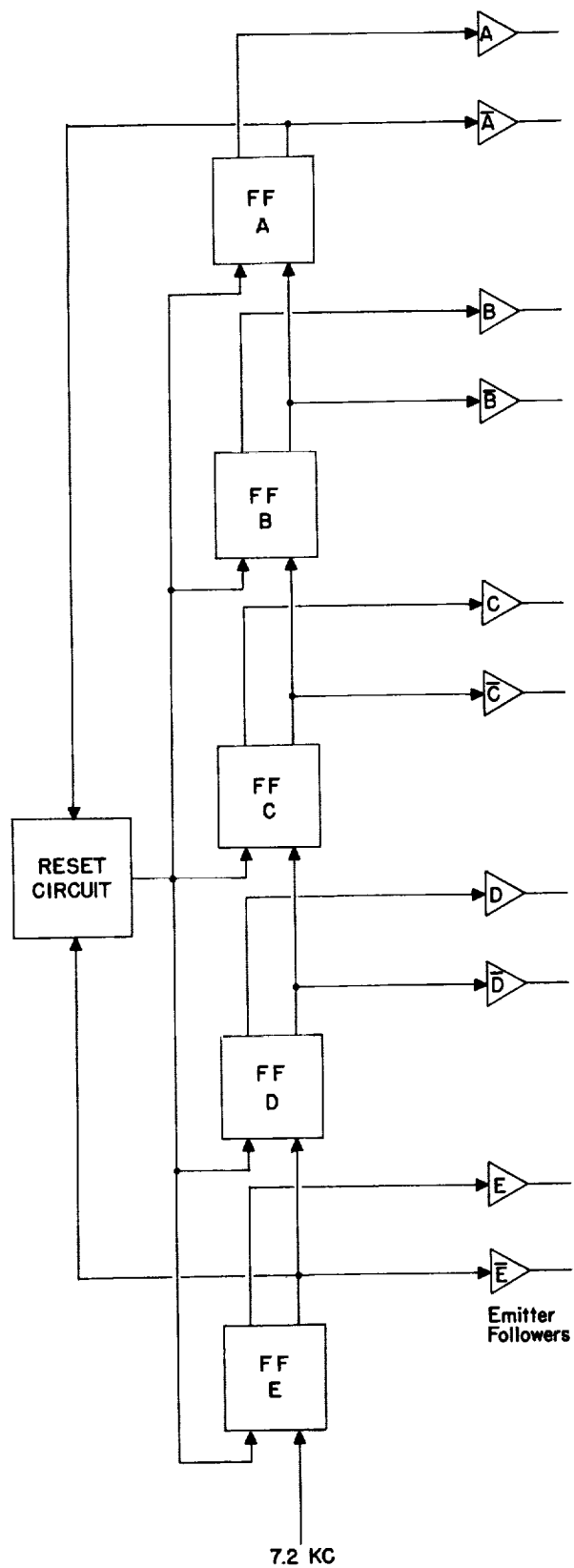


FIGURE I.
BLOCK DIAGRAM OF 0-17 COUNTER

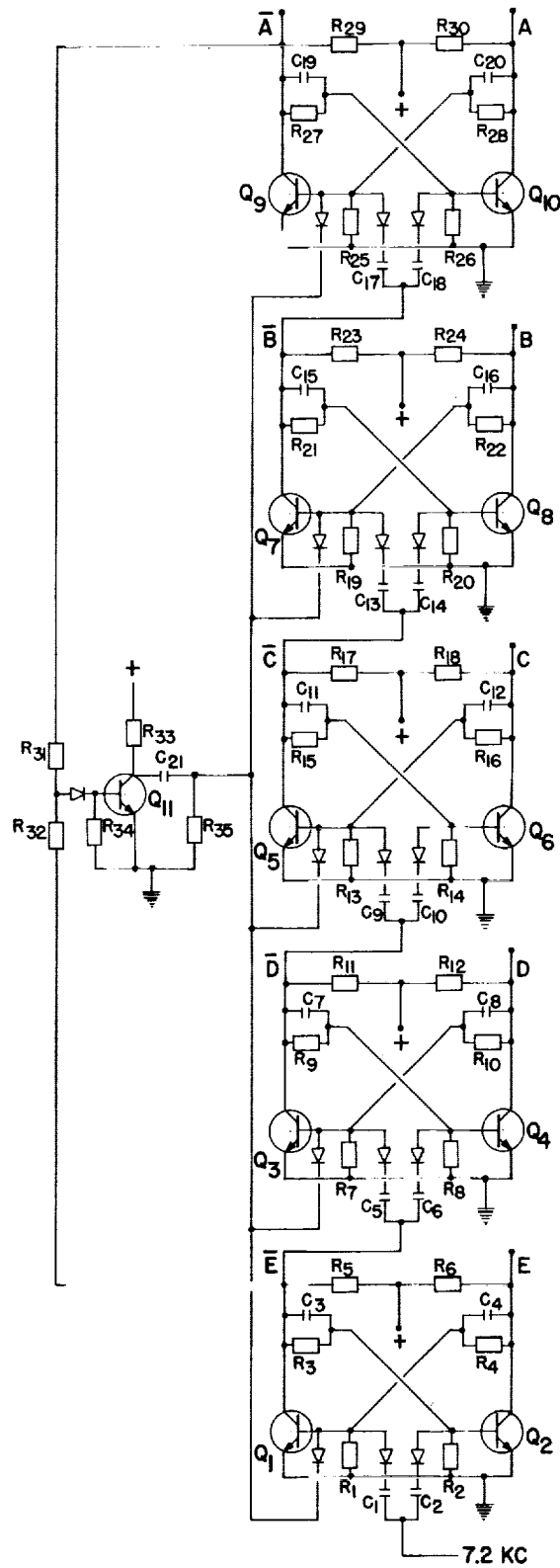


FIGURE 2.
BINARY COUNTER WITH RESET CIRCUIT
TO PRODUCE 0 TO 17 COUNT

A	B	C	D	E	m	f ₁	f ₆ ¹	f ₂	f ₇ ¹	f ₃	f ₈ ¹	f ₄	f ₉ ¹	f ₅
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
0	0	0	1	0	2	1	1	1	0	0	0	0	0	0
0	0	0	1	1	3	1	1	1	1	0	0	0	0	0
0	0	1	0	0	4	1	1	1	1	1	0	0	0	0
0	0	1	0	1	5	1	1	1	1	1	1	0	0	0
0	0	1	1	0	6	1	1	1	1	1	1	1	0	0
0	0	1	1	1	7	1	1	1	1	1	1	1	1	0
0	1	0	0	0	8	1	1	1	1	1	1	1	1	1
0	1	0	0	1	9	0	1	1	1	1	1	1	1	1
0	1	0	1	0	10	0	0	1	1	1	1	1	1	1
0	1	0	1	1	11	0	0	0	1	1	1	1	1	1
0	1	1	0	0	12	0	0	0	0	1	1	1	1	1
0	1	1	0	1	13	0	0	0	0	0	1	1	1	1
0	1	1	1	0	14	0	0	0	0	0	0	1	1	1
0	1	1	1	1	15	0	0	0	0	0	0	0	1	1
1	0	0	0	0	16	0	0	0	0	0	0	0	0	1
1	0	0	0	1	17	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

FIGURE 3.
TRUTH TABLE SHOWING THE CONDITION OF THE
FIVE FLIP-FLOPS AND THE NINE REQUIRED
FUNCTIONS TO PRODUCE THE OUTPUT WAVE WITH
STEPS AT 20° INTERVALS.

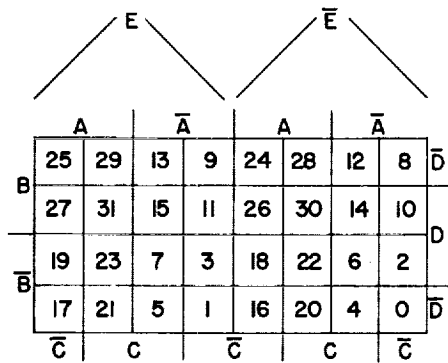


FIGURE 4.

SAMPLE VEITCH DIAGRAM FOR FIVE
VARIABLES SHOWING POSITION OF THE
MIN TERMS.

X	X			X	X		1
X	X			X	X		
X	X	1	1	X	X	1	1
	X	1	1	X	1	1	

$$f_1 = \bar{A}\bar{B} + \bar{A}C\bar{D}\bar{E}$$

X	X		1	X	X		1
X	X			X	X		
X	X	1	1	X	X	1	1
	X	1	1	X	1		

$$f_6 = \bar{B}C + \bar{B}D + \bar{A}B\bar{E} + B\bar{C}\bar{D}$$

X	X		1	X	X		1
X	X			X	X		1
X	X	1	1	X	X	1	1
	X	1		X	1		

$$f_2 = \bar{B}C + \bar{B}D + B\bar{C}\bar{E} + B\bar{C}\bar{D}$$

X	X		1	X	X		1
X	X		1	X	X		1
X	X	1	1	X	X	1	
	X	1		X	1		

$$f_7 = \bar{B}\bar{C} + \bar{B}C + \bar{B}D\bar{E}$$

X	X		1	X	X	1	1
X	X		1	X	X		1
X	X	1		X	X	1	
	X	1		X	1		

$$f_3 = \bar{B}C + \bar{B}\bar{C} + \bar{B}D\bar{E}$$

X	X	1	1	X	X	1	1
X	X		1	X	X		1
X	X	1		X	X	1	
	X	1		X			

$$f_8 = \bar{B}\bar{C} + \bar{B}D + \bar{B}C\bar{D} + \bar{B}C\bar{E}$$

X	X	1	1	X	X	1	1
X	X		1	X	X	1	1
X	X	1		X	X	1	
	X			X			

$$f_4 = \bar{B}\bar{C} + \bar{B}D + \bar{B}\bar{E} + \bar{B}C\bar{D}$$

X	X	1	1	X	X	1	1
X	X	1	1	X	X	1	1
X	X	1		X	X		
	X			X			

$$f_9 = B + C\bar{D}\bar{E}$$

X	X	1	1	X	X	1	1
X	X	1	1	X	X	1	1
X	X			X	X		
	X			1	X		

$$f_5 = B + A\bar{E}$$

FIGURE 5.

VEITCH DIAGRAMS OF NINE REQUIRED FUNCTIONS

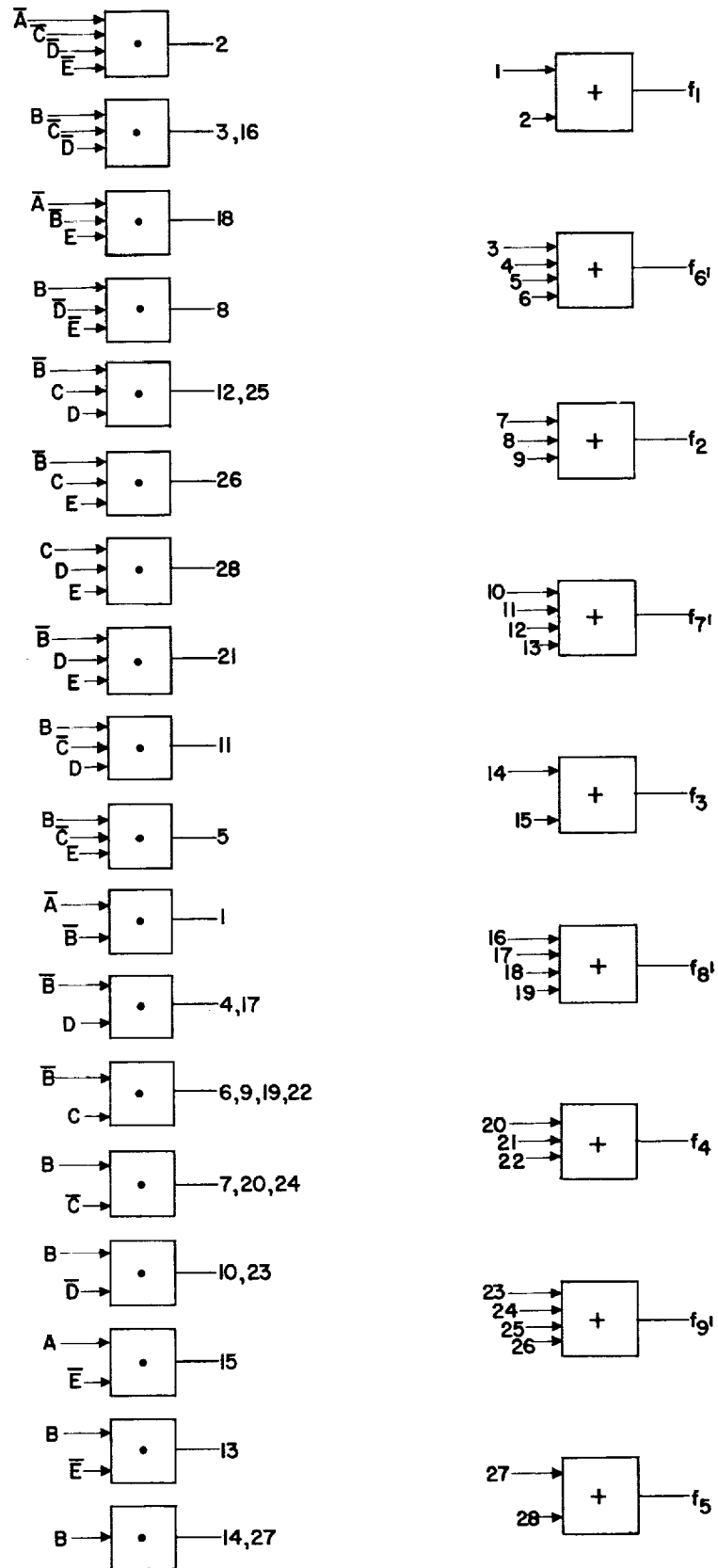


FIGURE 6.
BLOCK DIAGRAM OF THE DIODE LOGIC FOR FORMING
THE NINE REQUIRED FUNCTIONS.

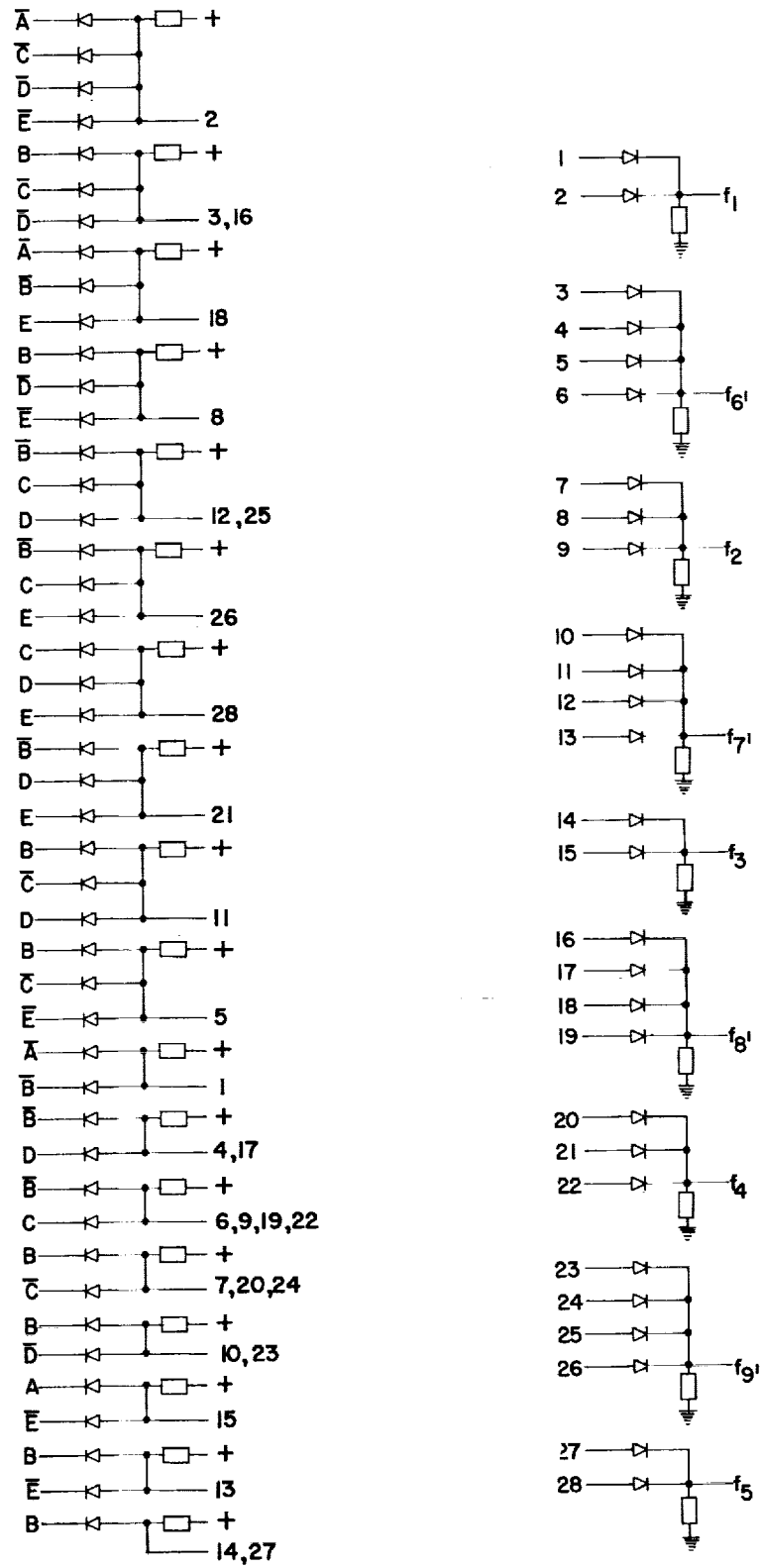


FIGURE 7
DIODE LOGIC

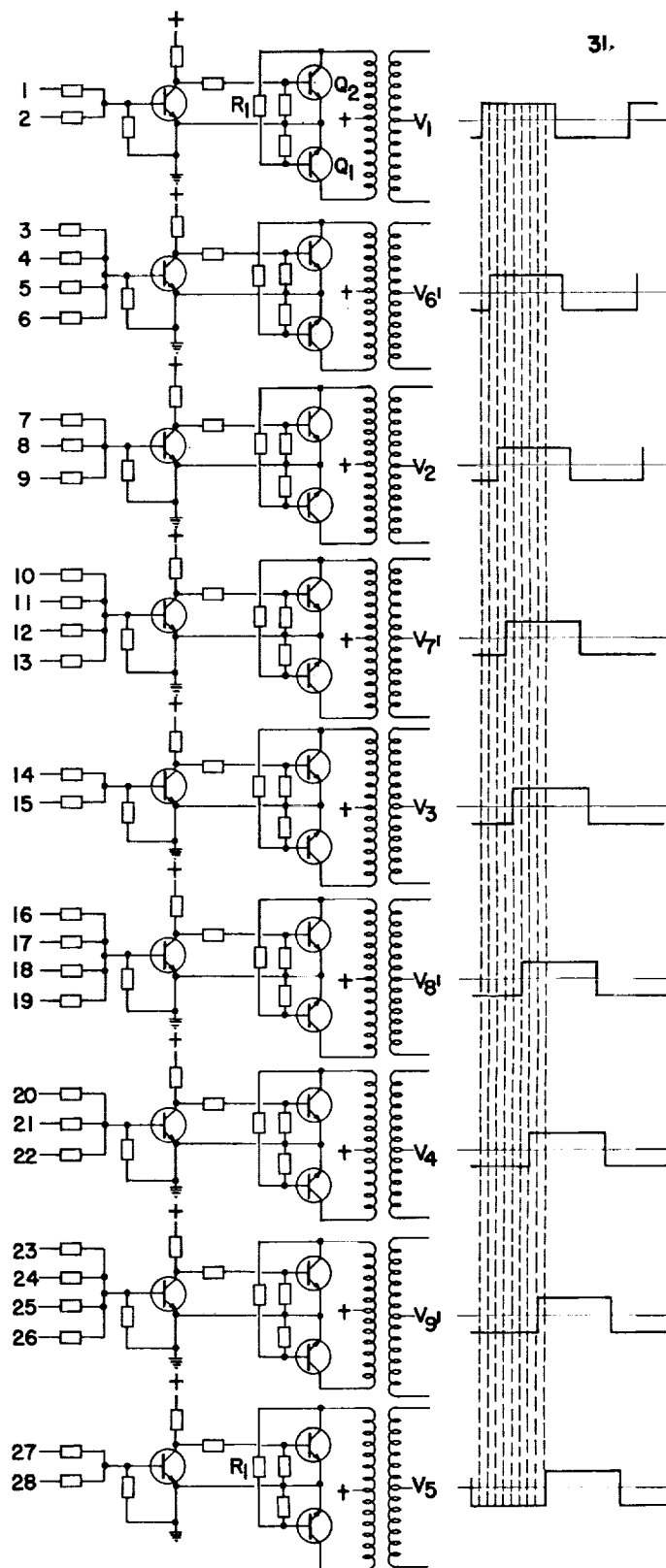
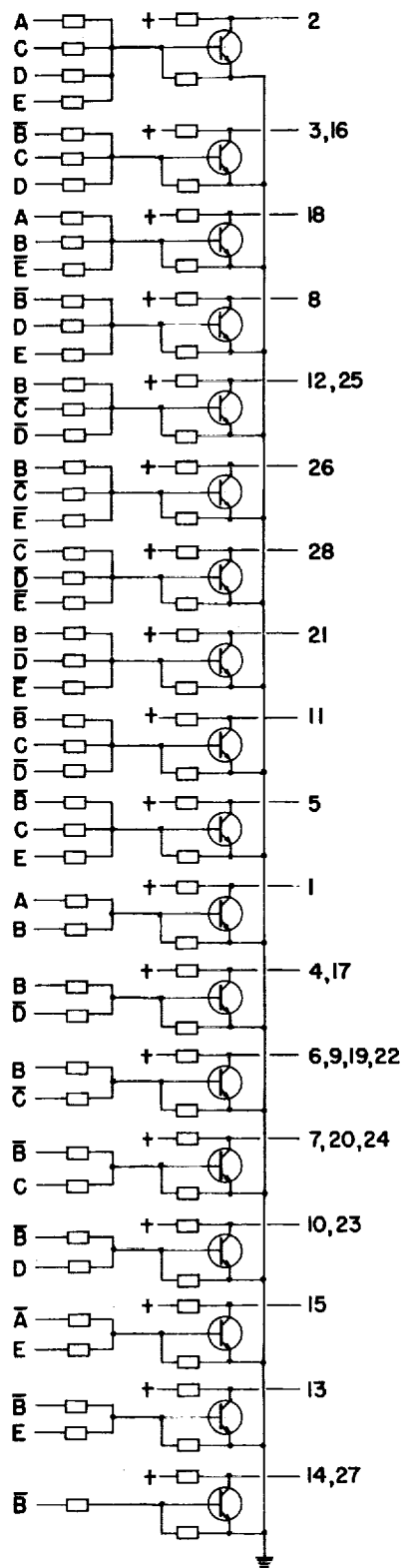


FIGURE 8.
TRANSISTOR LOGIC WITH PHASE INVERTER

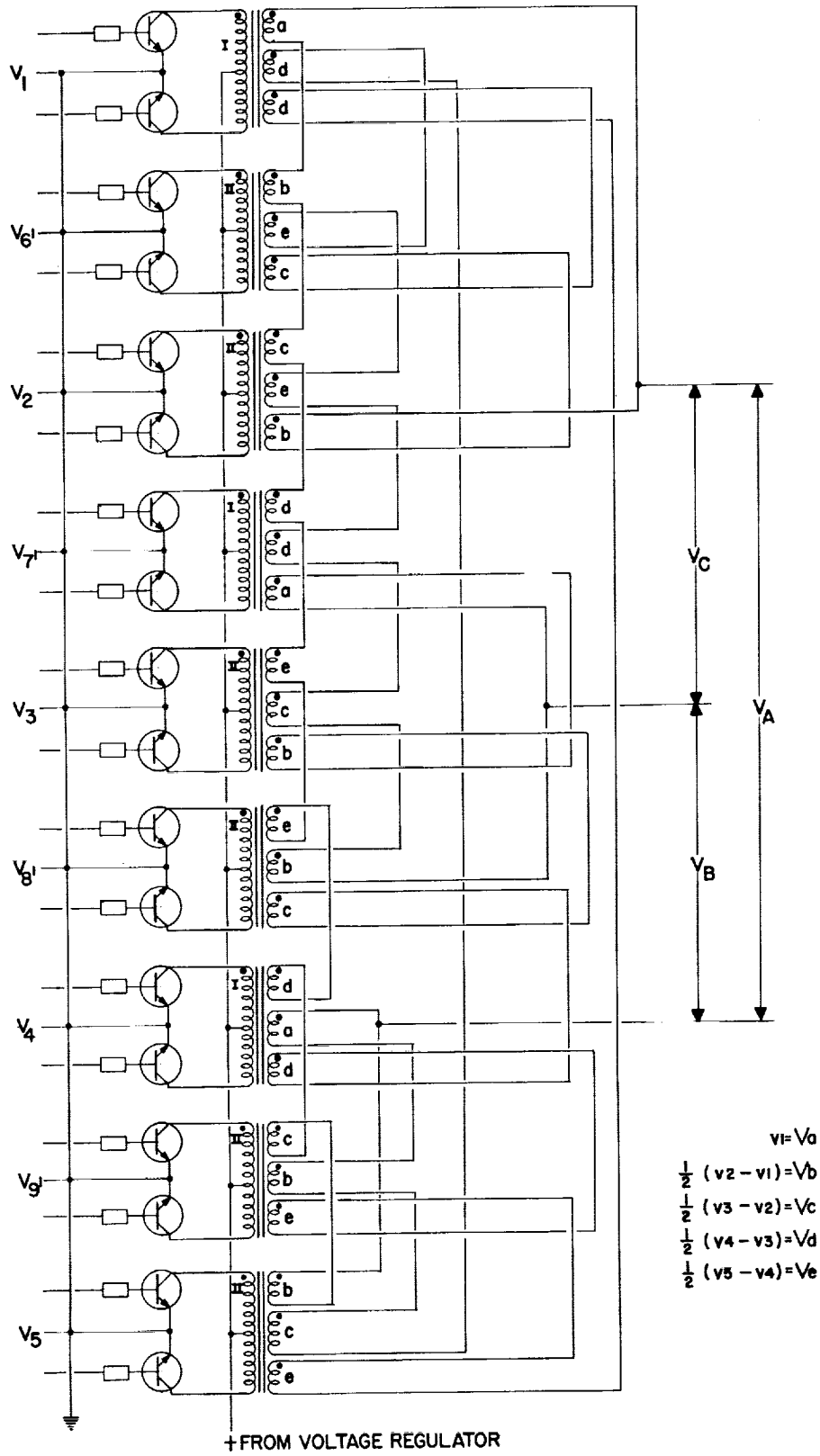


FIGURE 9.
POWER AMPLIFIERS WITH OUTPUT
TRANSFORMER CONNECTIONS.

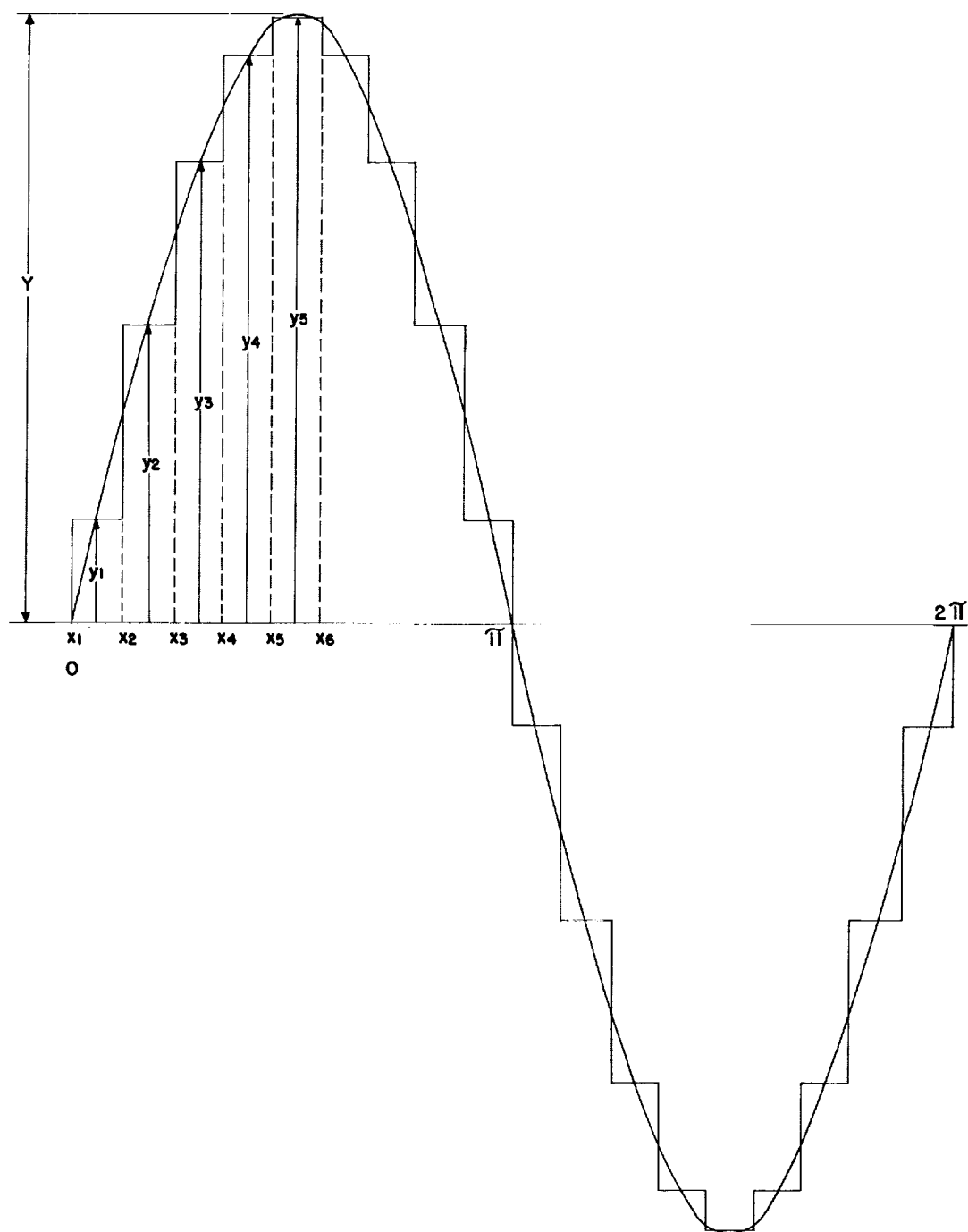


FIGURE 10.
STEPPED WAVE SUPERIMPOSED ON SINE WAVE

34

$$\begin{aligned}
 v_1 &= V_0 \\
 \frac{1}{2} (v_2 - v_1) &= V_b \\
 \frac{1}{2} (v_3 - v_2) &= V_c \\
 \frac{1}{2} (v_4 - v_3) &= V_d \\
 \frac{1}{2} (v_5 - v_4) &= V_e
 \end{aligned}$$

$$V_A = (V_0)_1 + (V_b)_6 + (V_c)_2 + (V_d)_7 + (V_e)_3 - (V_e)_8 - (V_d)_4 - (V_c)_9 - (V_b)_5$$

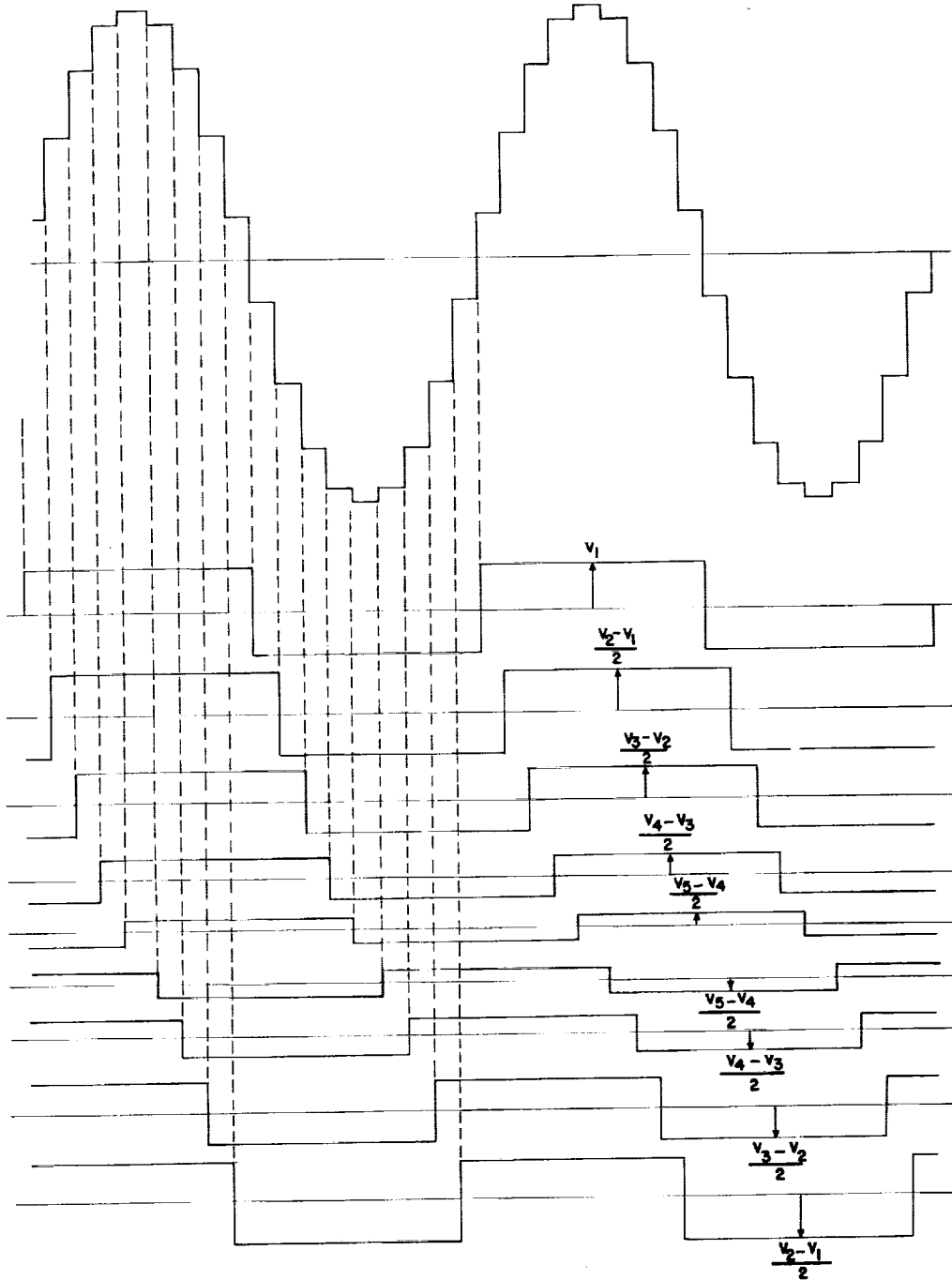


FIGURE II.
ADDITION OF NINE SQUARE WAVES TO FORM
REQUIRED STEPPED WAVE

A	B	C	D	E	m	f ₁	f ₂	f ₃	f ₄	f ₅	f ₆	f ₇	f ₈	f ₉	f ₁₀	f ₁₁	f ₁₂	f ₁₃	f ₁₄	f ₁₅
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	2	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	3	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	4	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	5	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	1	0	6	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	1	1	1	7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	0	8	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
0	1	0	0	1	9	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
0	1	0	1	0	10	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	1	1	11	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	1	0	0	12	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	1	1	0	1	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	1	1	0	14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	15	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	16	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	17	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	18	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	19	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	20	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	1	21	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
1	0	1	1	0	22	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
1	0	1	1	1	23	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
1	1	0	0	0	24	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
1	1	0	0	1	25	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	1	0	26	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	0	1	1	27	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
1	1	1	0	0	28	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	0	1	29	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

FIGURE 12.

TRUTH TABLE SHOWING THE CONDITION OF THE FIVE FLIP-FLOPS AND THE FIFTEEN REQUIRED FUNCTIONS TO PRODUCE THE OUTPUT WAVE WITH STEPS AT 12° INTERVALS

1	1			1	1		
1	X	1		1	X		
1	1			1	1		
1	1			1	1		

$$f_1 = A + BCDE$$

1	1			1	1		
1	X			1	X		
		1		1	1		1
		1		1	1		1

$$f_6 = AB + AC + \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}\bar{D}\bar{E}$$

1	1			1	1		
1	X			1	X		
		1	1			1	1
		1	1			1	1

$$f_{11} = \bar{A}\bar{B} + ABC + ABD + ABE + \bar{A}\bar{C}\bar{D}$$

1	1			1	1		
1	X			1	X		
1	1			1	1		
1	1			1	1		

$$f_2 = A + \bar{B}\bar{C}\bar{D}\bar{E}$$

1	1			1	1		
1	X			1	X		
		1		1	1		1
		1		1	1		1

$$f_7 = AB + ACD + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}\bar{D}\bar{E}$$

	1			1	1		
1	X			1	X		
		1	1			1	1
		1	1			1	1

$$f_{12} = \bar{A}\bar{B} + ABC + ABD + \bar{A}\bar{C}\bar{D} + \bar{A}\bar{C}\bar{E}$$

1	1			1	1		
1	X			1	X		
1	1			1	1		
1	1			1	1		

$$f_3 = AB + AC + AD + AE + \bar{A}\bar{B}\bar{C}\bar{D}$$

1	1			1	1		
1	X			1	X		
		1		1	1		1
		1		1	1		1

$$f_8 = AB + ACD + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{B}\bar{E}$$

	1			1	1		
1	X			1	X		
		1	1			1	1
		1	1			1	1

$$f_{13} = \bar{A}\bar{B} + \bar{A}\bar{C} + ABC + \bar{B}\bar{C}\bar{D}\bar{E}$$

1	1			1	1		
1	X			1	X		
1	1			1	1		
		1		1	1		1

$$f_4 = AB + AC + AD + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D}\bar{E}$$

1	1			1	1		
1	X			1	X		
		1		1	1		1
		1		1	1		1

$$f_9 = AB + \bar{A}\bar{B} + \bar{B}\bar{C}\bar{D}\bar{E}$$

	1			1	1		
	X			1	X		
		1	1			1	1
		1	1			1	1

$$f_{14} = \bar{A}\bar{B} + \bar{A}\bar{C} + ABC + \bar{A}\bar{D}\bar{E}$$

1	1			1	1		
1	X			1	X		
1	1			1	1		
		1		1	1		1

$$f_5 = AB + AC + ADE + \bar{A}\bar{B}\bar{C}$$

1	1			1	1		
1	X			1	X		
		1		1	1		1
		1		1	1		1

$$f_{10} = AB + \bar{A}\bar{B} + \bar{B}\bar{C}\bar{D}\bar{E}$$

	1			1	1		
	X			1	X		
		1	1			1	1
		1	1			1	1

$$f_{15} = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}\bar{E}$$

FIGURE 13.
VEITCH DIAGRAMS OF FIFTEEN REQUIRED FUNCTIONS

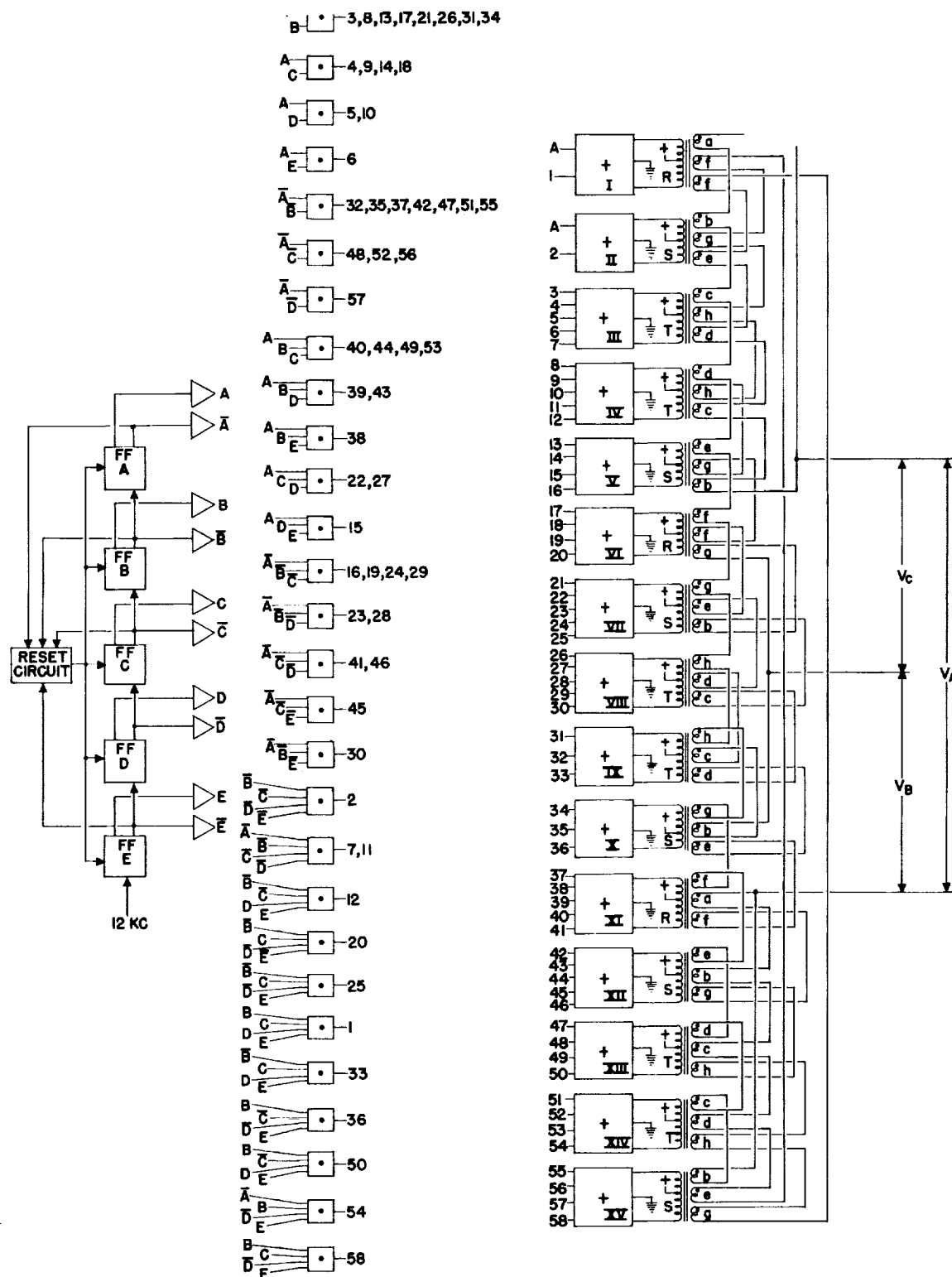


FIGURE 14.
BLOCK DIAGRAM OF COUNTER AND LOGIC SHOWING
OUTPUT TRANSFORMER CONNECTIONS FOR STATIC
INVERTER WITH STEPS AT 12° INTERVALS ON THE
OUTPUT WAVE

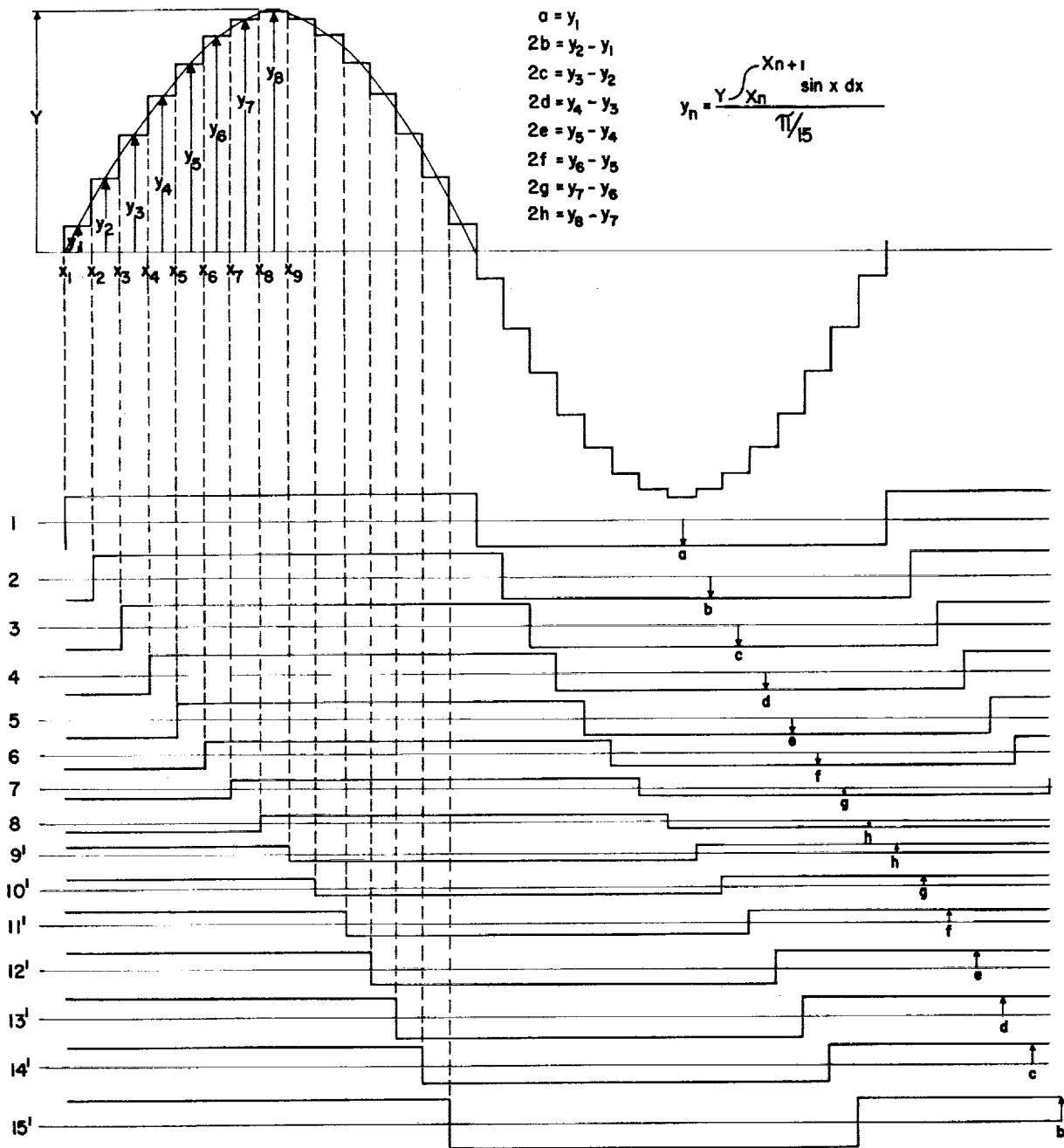


FIGURE 15.
ADDITION OF FIFTEEN SQUARE WAVES TO FORM
REQUIRED STEPPED WAVE

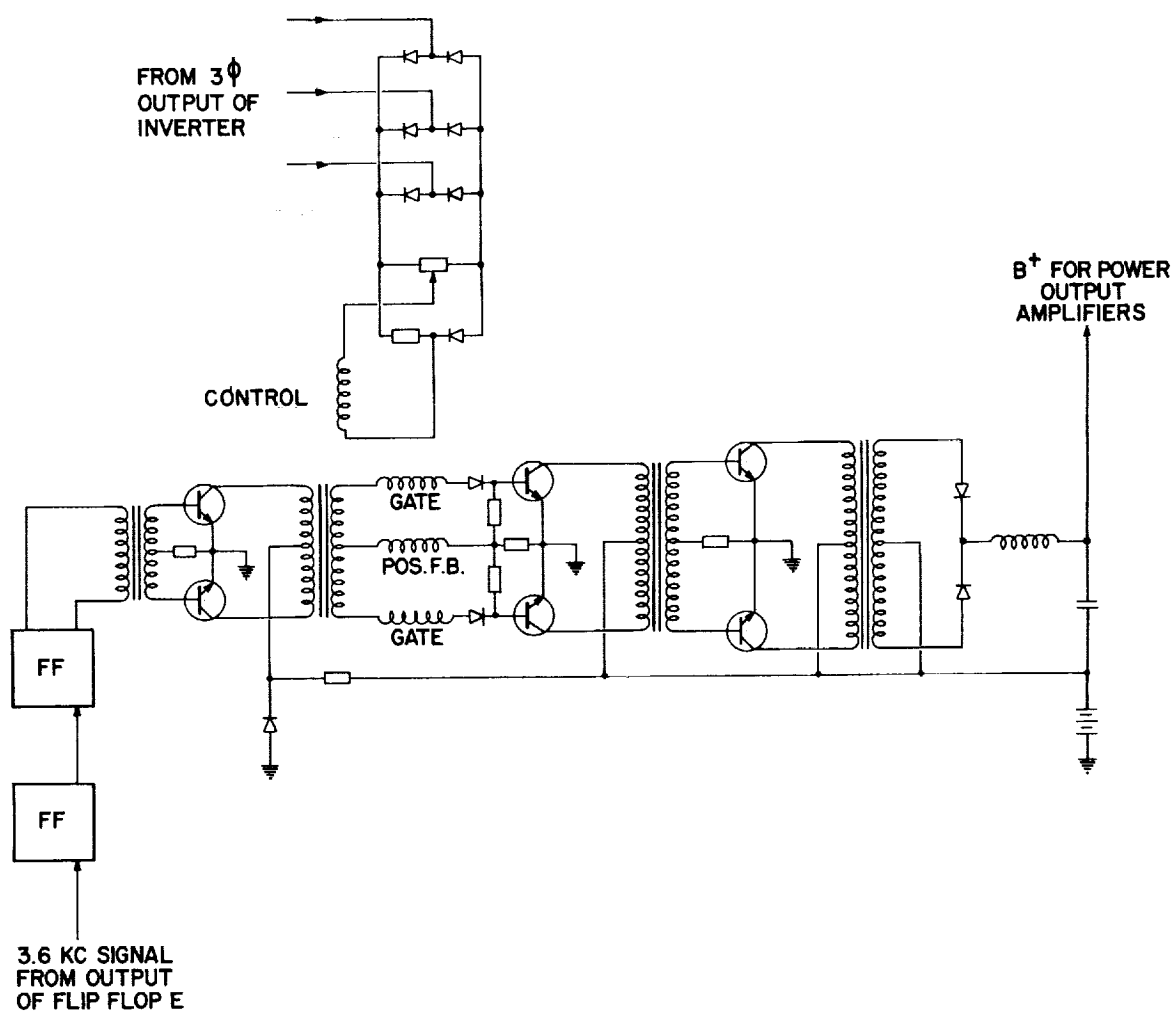


FIGURE 16.
D.C. VOLTAGE REGULATING ARRANGEMENT

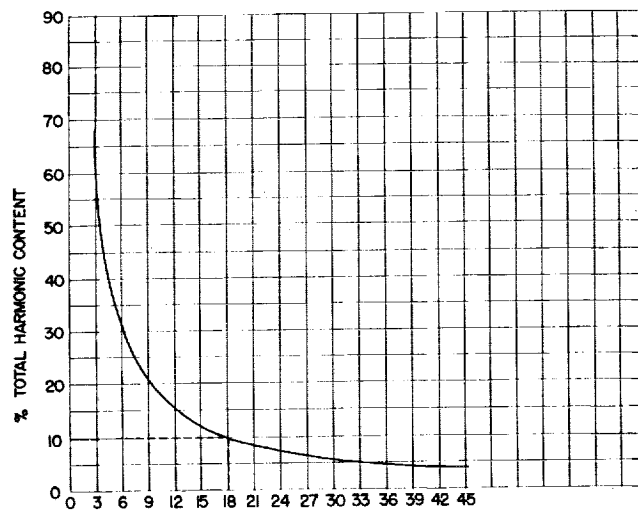


FIGURE 17. PERCENT TOTAL HARMONIC DISTORTION AS A FUNCTION OF THE NUMBER OF STEPS ON THE OUTPUT WAVE

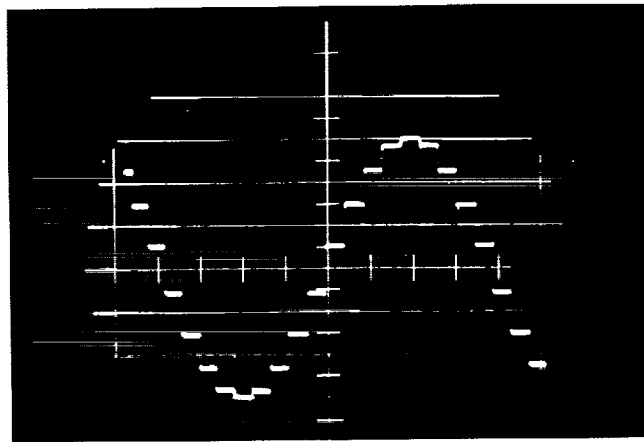


FIGURE 18. OUTPUT VOLTAGE WAVE

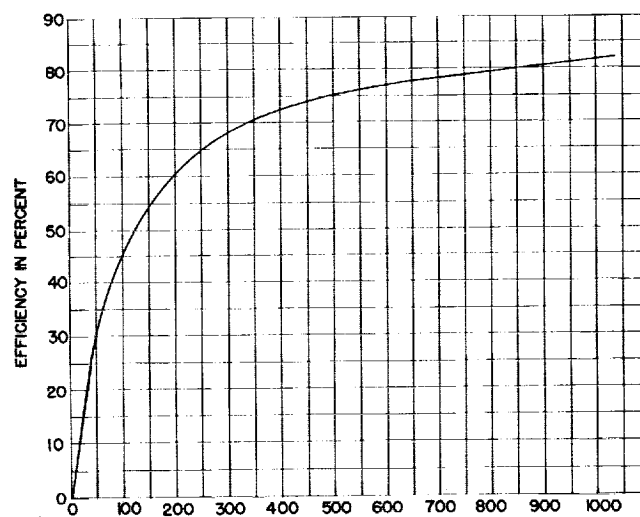


FIGURE 19. PERCENT EFFICIENCY AS A FUNCTION OF LOAD

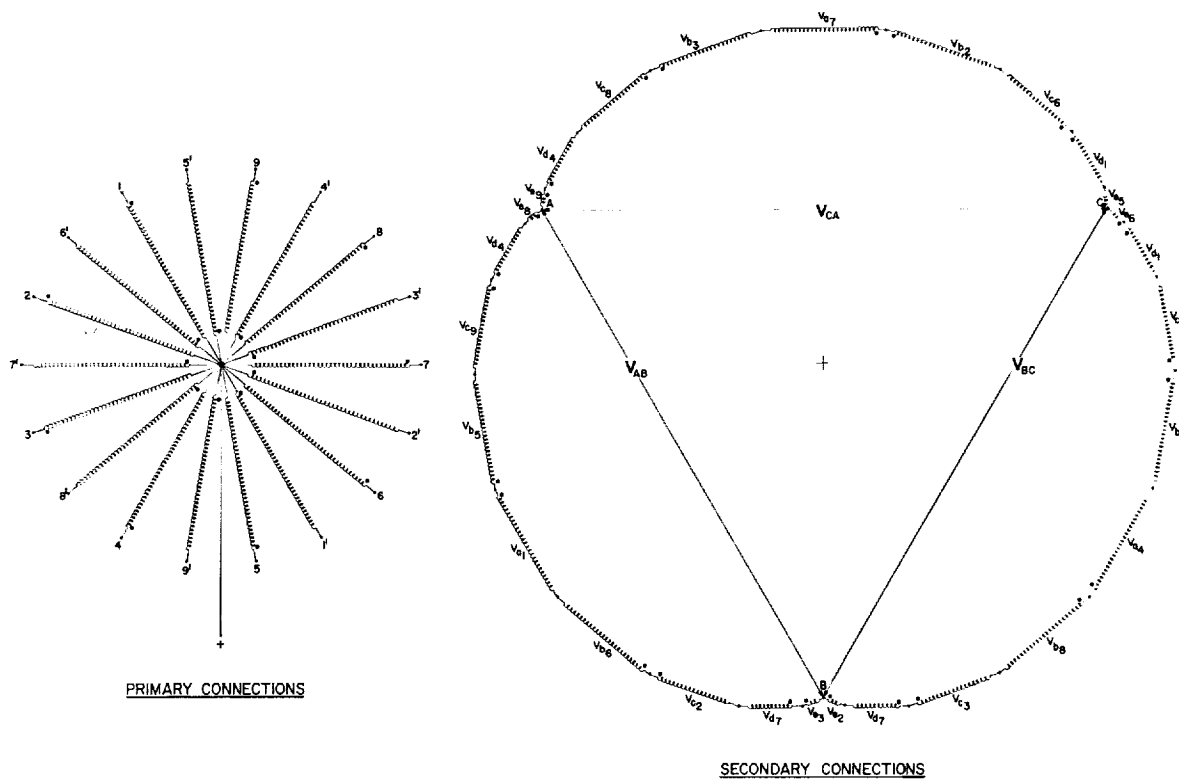
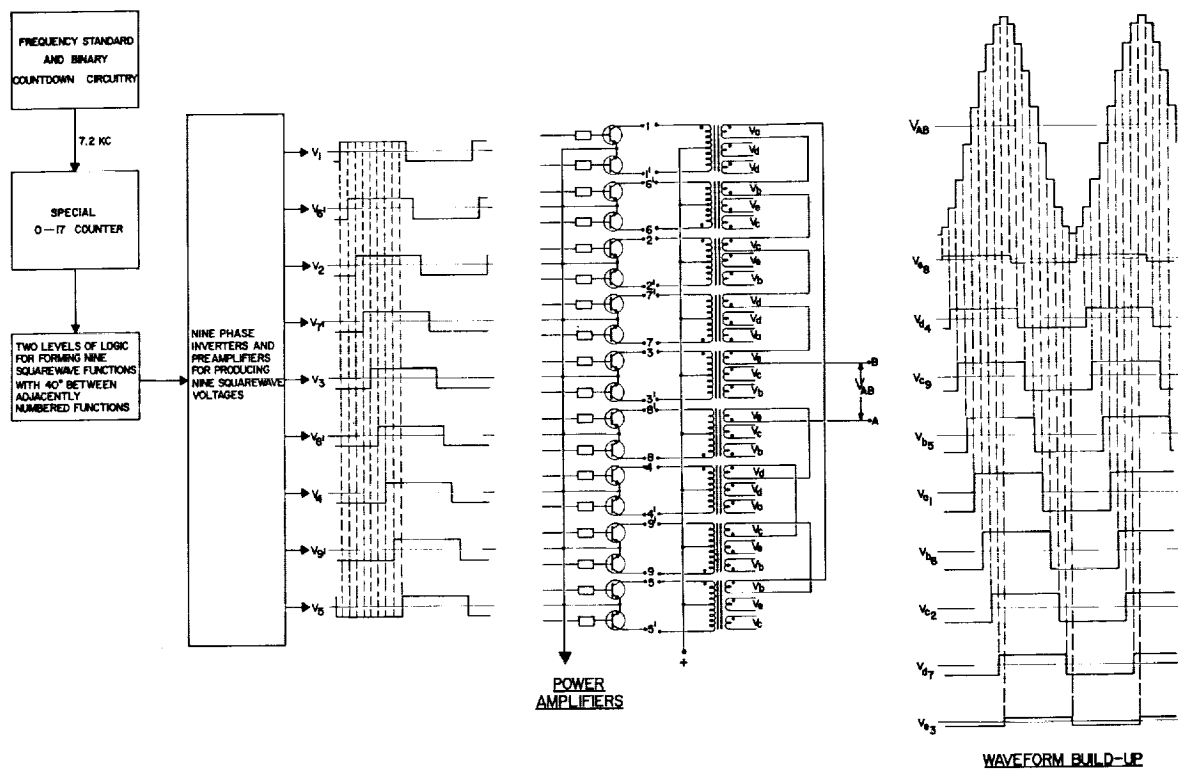


FIGURE 20 THREE PHASE STATIC INVERTER

<p>NASA TN D-602 National Aeronautics and Space Administration. ADVANCED STATIC INVERTER UTILIZING DIGITAL TECHNIQUES AND HARMONIC CANCELLATION. Dorrance L. Anderson, Albert E. Willis, and Carl E. Winkler. May 1962. 41p. OTS price, \$1.25. (NASA TECHNICAL NOTE D-602)</p> <p>Various approaches have been made toward the development of static inverters. This report describes certain techniques that lead to a highly efficient unit that is smaller and lighter than static inverters of comparable rating. The output wave shape approaches a sine wave and is made up of steps, thus eliminating the necessity of a wave-shaping filter. The circuitry consists of a frequency standard, binary countdown flip-flops, logic elements, power amplifiers, and output transformers that are uniquely interconnected. A magnetic amplifier type of voltage regulator is used.</p>	<p>I. Anderson, Dorrance L. II. Willis, Albert E. III. Winkler, Carl E. IV. NASA TN D-602</p> <p>(Initial NASA distribution: 2, Aerodynamics, missiles and space vehicles; 3, Aircraft; 19, Electronics.)</p>	NASA
<p>NASA TN D-602 National Aeronautics and Space Administration. ADVANCED STATIC INVERTER UTILIZING DIGITAL TECHNIQUES AND HARMONIC CANCELLATION. Dorrance L. Anderson, Albert E. Willis, and Carl E. Winkler. May 1962. 41p. OTS price, \$1.25. (NASA TECHNICAL NOTE D-602)</p> <p>Various approaches have been made toward the development of static inverters. This report describes certain techniques that lead to a highly efficient unit that is smaller and lighter than static inverters of comparable rating. The output wave shape approaches a sine wave and is made up of steps, thus eliminating the necessity of a wave-shaping filter. The circuitry consists of a frequency standard, binary countdown flip-flops, logic elements, power amplifiers, and output transformers that are uniquely interconnected. A magnetic amplifier type of voltage regulator is used.</p>	<p>I. Anderson, Dorrance L. II. Willis, Albert E. III. Winkler, Carl E. IV. NASA TN D-602</p> <p>(Initial NASA distribution: 2, Aerodynamics, missiles and space vehicles; 3, Aircraft; 19, Electronics.)</p>	NASA
<p>NASA TN D-602 National Aeronautics and Space Administration. ADVANCED STATIC INVERTER UTILIZING DIGITAL TECHNIQUES AND HARMONIC CANCELLATION. Dorrance L. Anderson, Albert E. Willis, and Carl E. Winkler. May 1962. 41p. OTS price, \$1.25. (NASA TECHNICAL NOTE D-602)</p> <p>Various approaches have been made toward the development of static inverters. This report describes certain techniques that lead to a highly efficient unit that is smaller and lighter than static inverters of comparable rating. The output wave shape approaches a sine wave and is made up of steps, thus eliminating the necessity of a wave-shaping filter. The circuitry consists of a frequency standard, binary countdown flip-flops, logic elements, power amplifiers, and output transformers that are uniquely interconnected. A magnetic amplifier type of voltage regulator is used.</p>	<p>I. Anderson, Dorrance L. II. Willis, Albert E. III. Winkler, Carl E. IV. NASA TN D-602</p> <p>(Initial NASA distribution: 2, Aerodynamics, missiles and space vehicles; 3, Aircraft; 19, Electronics.)</p>	NASA
<p>NASA TN D-602 National Aeronautics and Space Administration. ADVANCED STATIC INVERTER UTILIZING DIGITAL TECHNIQUES AND HARMONIC CANCELLATION. Dorrance L. Anderson, Albert E. Willis, and Carl E. Winkler. May 1962. 41p. OTS price, \$1.25. (NASA TECHNICAL NOTE D-602)</p> <p>Various approaches have been made toward the development of static inverters. This report describes certain techniques that lead to a highly efficient unit that is smaller and lighter than static inverters of comparable rating. The output wave shape approaches a sine wave and is made up of steps, thus eliminating the necessity of a wave-shaping filter. The circuitry consists of a frequency standard, binary countdown flip-flops, logic elements, power amplifiers, and output transformers that are uniquely interconnected. A magnetic amplifier type of voltage regulator is used.</p>	<p>I. Anderson, Dorrance L. II. Willis, Albert E. III. Winkler, Carl E. IV. NASA TN D-602</p> <p>(Initial NASA distribution: 2, Aerodynamics, missiles and space vehicles; 3, Aircraft; 19, Electronics.)</p>	NASA

